AR7030 Circuit Description

1) RF and IF section

1.0 Frequency configuration

The AR7030 is a dual-conversion superheterodyne receiver, using intermediate frequencies of 45MHz and 455kHz in its two IF stages. RF signals are converted to 45MHz by the local oscillator signal (LO) which is tuned from 45.00000MHz to 77.01672MHz to give receiver coverage of 00.000kHz to 32.01672MHz. The local oscillator is tuned in 2.655Hz steps. The LO is offset by approximately +/- 1.4kHz in SSB mode, the exact offset being determined from the filter offset derived from the filter calibration table. It is also offset up to +/- 4.2kHz during PBS operation.

Conversion between the two IF's is by the fixed heterodyne oscillator signal (HET) running at 44.545MHz.

In SSB, AM, CW, Sync and Data modes audio is derived by mixing the final IF with a carrier reinsertion signal. The frequency of this reflects any offset generated by the LO and is nominally 455kHz +/- the filter offset, PBS and BFO offset.

1.1 Whip Amplifier

The whip amplifier is only present in circuit when the Antenna Select switch is set to the Whip position. The JFET device (Q15) provides a high input impedance to give good results at low frequencies with the capacitive load of a whip or a short wire aerial. The drain output of Q15 is fed into the input of matching transformer L6 which provides impedance coupling for both the whip amplifier and long wire aerial input.

1.2 Attenuator and RF Pre-amp

Front end attenuation is controlled by RL1 and RL2 and their associated resistor networks R26-R29. They provide 0dB, 20dB and 40dB of attenuation as well as switching for the VHF Option through J7. The RF Pre-amp consists of Q16 and matching transformers L17 and L18. This provides 10dB of gain. It is switched in and out of circuit by RL4 and when used in conjunction with the attenuator settings provides the specified levels of RF gain -40dB, -30dB, -20dB, -10dB, 0dB and +10dB.

1.3 Front end Filters

Frequencies below 1.7MHz pass through a low-pass filter L10. L11 and C25-27. Frequencies above 1.7MHz pass through a high-pass filter L8. L9 and C22-24. All signals pass through the 30MHz low-pass filter L12-15 and C28-33. These filters help reduce spurious mixing effects caused by strong signals outside the band being received.

A DC path is maintained through all the switching relay contacts and a small current is passed through them to prevent oxidation, this is known as "contact wetting".

1.4 1st Mixer and 1st IF

An SD5400 DMOSFET mixer (Q17) and JFET buffer amp (Q18 and Q19) are used to convert the RF signal to the first IF at 45MHz. Balun L21 provides a balanced signal feed and L22 provides a balanced LO feed. The balanced output is matched to the 45MHz crystal roofing filters X2A and X2B by a tuned transformer L26. In this configuration the mixer provides a small amount of gain to ensure adequate sensitivity and offers more than 100dB intermodulation-free dynamic range.

1.5 2nd Mixer and 2nd IF

An SL6440 gilbert cell mixer (Q20) is used to convert to the 2nd IF at 455kHz. The 15kHz bandwidth of the roofing filters in the 1st IF reduces the dynamic range requirement of the 2nd mixer. The output from the 2nd mixer is applied directly to the main group of IF filters X3-X8. All the filters are centred on 455kHz and are switched by Q21-24, triple two channel multiplexers. Depending on the required bandwidth one of the IF filter select lines (FS1-6) goes to +5V. Output for the Noise Blanker Option is available on J10. After filtering the signal passes to the TDA1572 (Q30) where the main IF amplification and AGC control takes place. The output passes through a buffer amp (Q31) and on to one of two IF tail filters switched by Q32, the spare multiplexer being used to ground the output of the unused filter. The automatic filter selection at this point is dependant on which of the main filters are selected.

1.6 AGC system

AGC is provided primarily by controlling the gain of the main IF amplifier Q30. Signal level output is available on pin 8 and AGC input control on pin 7. The AGC system comprises Q34, Q35A, Q35B and Q36A and various switching lines.

- The AM line goes to +5V in AM, Sync and FM mode and switches Q36A to provide average signal level AGC. For SSB modes the circuit responds to peak signals.
- The MAN line goes +5V when the AGC is switched off. This turns Q34A on and disables the signal input into the AGC system causing the receiver to operate at full gain.
- The AS1 line goes +5V when the AGC is switched off or to fast. This alters the AGC time constant through R99.
- The AS2 line goes +5V when the AGC in switched off, fast or medium. This alters the AGC time constant through R100. When the AGC is set to slow, both AS1 and AS2 go to 0V.

- The AGC line connected to the control system and is bi-directional. An A/D converter provides S-Meter data for the control system and a D/A converter allows the microprocessor controlled RF gain control to set a minimum voltage on to the AGC line and thereby provide manual RF gain control.

If the control system detects signal strengths in excess of S9 +40 and the RF gain is set to AUTO the control system will automatically switch in front end RF attenuation using the relays.

1.7 Detectors

The IF signal is split two ways for detection, however both detectors operate at the same time in all modes and the choice of detection mode is made by the audio control IC, Q38.

For FM detection the signal is fed to the MC3357 (Q33) where it passes through the limiting amps to the quadrature FM detector X12 and out through pin 9 to the audio control IC, Q38.

For AM, Sync, SSB, CW and Data modes, detection is carried out in the product detector NE612A (Q37). The incoming IF signal is mixed with the generated carrier and the resultant audio passes out through pin 5 to the audio control IC (Q38). The carrier signal for the product detector is provided by the DDS system in SSB, CW and Data modes, and from the limiting amplifer in Q33 for AM mode.

1.8 Synchronous AM

Synchronous AM operates in a similar way to the SSB modes except that the DDS carrier frequency is offset by about 20kHz and then mixed with a 20kHz VCO (Q41) giving the required 455kHz injection. Filter X13 removes unwanted mixing sidebands. The VCO frequency is controlled to maintain phase lock between the IF and the injected carrier using the spare mixer in Q33.

The operation of the system is monitored by the control processor when in AUTO mode - error voltages developed on the OFS and SLK lines are used to maintain sync lock. VR2 aligns the sync offset voltage and VR3 tunes the VCO. The SBW line controls the narrow / wide switching of the Sync PLL system. The SYN line goes low when Sync mode is selected to turn on the VCO.

2) AF Stage

The hub of the audio control system is the TDA9860, Q38. This is a stereo audio pre-amp IC and is controlled by the microprocessor via an I^2C bus. Control is available for three inputs, volume, bass, treble and three outputs - all in stereo. The main output is combined to mono and fed to the TDA1904 (Q40) which is the main audio amp feeding the internal loudspeaker and external loudspeaker socket. The main output is also fed to Q39A and Q39B which provides independent stereo headphone amplification. The main audio feed to the internal or external loudspeaker is isolated if a plug is inserted in the headphone socket. The aux output is fed to Q39C and Q39D which provides independent stereo line output to the rear aux socket.

3) Power Supply

Nine supply rails are used in the receiver

- +5C is an permanently active, unswitched 5V supply powering everything that requires power when the unit is switched off but still connected to a supply. It feeds the control system, the rear IR sensor, the I/O expanders, the Ref oscillator, multiplier (Q46) and the mixer driver (Q57). The supply is provided by a 5V regulator Q74 from the main supply input. All other supplies are inactive until the unit is switched on.

- B+ operates at about 1V less than the DC supply input and feeds the aux relay, the aux and remote supply feed, the audio option, the DC-DC converter, some of the AGC system, the headphone and line output amps and the main audio amp. It is used as the main switched supply in the receiver and is controlled by Q70.

- B+S is derived from B+ and is smoothed and decoupled through L65. It feeds the front end switching relays, the RF pre-amp and the 1st mixer FET's Q18 and Q19.

- +8 is an 8V supply derived from B+ through regulator Q73. It feeds the whip amplifier, the 1st mixer bias, the 2nd mixer, the IF stages, the local oscillator, the AGC and Sync op-amp (Q35) and the PLL integrator Q62.

- +5 is a 5V supply derived from the +5C line and is switched through Q78 when B+ is active. It feeds both DDS systems, the PLL prescaler and phase comparator, the Sync system, the AGC time constants, the product detector and the IF filter select IC's Q21-Q24.

- +20 is a nominal 20V, low current supply and is obtained from a DC-DC converter (Q64) by voltage doubling and rectifying the high level DDS sine wave output. It feeds the PLL voltage control line.

- -7 is a nominal -ve 7V, low current supply and is obtained by rectifying the high level DDS sine wave output. It provides the -ve bias for the first mixer.

- -3 is a nominal -ve 3V supply and is derived from a potential divider off the -7 supply. It provides -ve bias for the filter switching multiplexers.

- BLA and BLC form a constant current current feed to the LCD backlight LED’s. This supply is derived from the voltage drop across the 5V regulator, Q74.

The power supply is initially switched on by the PWR line from the control unit going low and switching Q71, Q72 and the main supply control transistor Q70. Once the control system has stabilised the OPR line out of the I/O expander Q81 goes high and maintains control of Q72.

4) Frequency Synthesiser

4.1 Reference Oscillator

The frequency stability and frequency accuracy of the entire set, except for the real time clock, is dependant on the Reference Oscillator. It consists of a temperature compensated xtal oscillator (TCXO) running at 11.13625MHz and a buffer stage Q46. It supplies a reference to the CPU, DDS systems and Het multiplier.

4.2 Heterodyne Multiplier

The Heterodyne injection signal is derived from the TCXO and multiplied by Q46 producing a comb of strong harmonics. The fourth harmonic at 44.545MHz is selected by the tank circuit TC2, C64 and L29 and fed into the 2nd Mixer, Q20.

4.3 Carrier DDS

The carrier signal is produced digitally by an HSP45102 DDS IC (Q47) and converted to a pure sine wave of about 1V P-P using the resistor ladder network R154 - R165. This IC is programmed by the CLK, DAT and STC lines directly out of the CPU. The carrier is centred around 455kHz for CW, SSB and Data modes and 434.71kHz for Sync mode, the frequency varies slightly to reflect the mode, selected filter, BFO and PBS offset and during Sync tune. This signal is fed into the Sync system IC, Q41.

4.4 Local DDS

The local signal is produced by a second HSP45102 DDS IC (Q48), buffered in the Hex Flip/Flops (Q49 and Q50), converted in the resistor ladder network R166 to R189 and further buffered by Q51 to produce a pure sine wave of about 3V P-P. This IC is programmed by the CLK, DAT and STL lines directly out of the CPU. The Local DDS tunes from about 87.89kHz to 150.42kHz +/- all the various offsets, and provides the reference signal for the PLL system phase comparator on pin 3. It also provides the reference for the VHF Option on J9 and the signal to drive the DC-DC converter.

4.5 Local Oscillator

The local oscillator is based around a J310 FET grounded gate VCO (Q55),. It is tuned by two tank circuits, L51/C163 and L50/C155. Both these circuits are padded with extra capacitance C153/C154 and C161/C162 as the set is tuned down in frequency. The switching is controlled by two lines LR1 and LR2 feeding switching transistors Q52 and Q53. The table below shows the frequency switching configuration.

Frequency range	LR1	LR2
0.000kHz - 3.95858MHz	High	High
3.91508MHz - 9.52672MHz	Low	High
9.48321MHz - 17.18289MHz	High	Low
17.13938MHz - 32.01672MHz	Low	Low

It can be seen that there is hysteresis built into the change over points. This is to prevent the characteristic spot frequency "pop" that is normal when a PLL changes ranges. The oscillator is fine-tuned by two varicap diodes D30 and D31 whose capacitance is controlled by the VCV line generated by the phase comparator and appearing at TP5. The output of the local oscillator is buffered by Q56, another grounded gate J310 FET, before being fed into the mixer driver Q57.
The HF line is switched low during VHF operation to switch off the Local Oscillator and Het multiplier - normally at HF it is at +5V.

4.6 Mixer Driver

The mixer driver Q57 provides the high level drive for the first mixer appearing at LO and also the low level feed into the prescaler Q58.

4.7 Prescaler

The prescaler consists of a 74AC74 (Q58) 2-bit counter and a 7-bit binary ripple counter (Q59). These are used to divide the local oscillator output by 512 and provide a 5V P-P square wave PLL IF of 87.89kHz to 150.42kHz to feed into the phase comparator, Q63.

4.8 Phase comparator

The phase comparator 74HC9046 (Q63) compares the phases of the PLL IF with the Local DDS reference signal and produces a current output at pin 13. This is integrated and filtered by Q60, Q61 and Q62 to produce the VCV voltage to tune the local oscillator, completing the loop of the PLL. The phase comparator also generates an unlock signal if the loop becomes unlocked. This appears at pin 2 and becomes the PLK line feeding the CPU. During an unlock state the line goes to +5V, mutes the audio and disables the S-meter display via the CPU.

5) Control unit

At the centre of the control system is the CPU (Q5) an 89C52. This IC contains a program specific to the AR7030 and provides an interface between the operator and the receiver's electronics.

- It accepts commands from the three rotary encoders S1 -S3, the nine push buttons S4 - S12 and drives the display Q10 on the parallel bus - D0 to D7, DEN, DRD and DRS

- It monitors voltages from the AGC and Sync systems and controls the manual IF gain via the A/D - D/A converter (Q9), reads data in and out of the RTC/RAM (Q6), EEPROM (Q7) and optional EEPROM (Q8) using the control I^2C bus - SC1 and SD1.

- Audio control via Q38 and receiver control via a 24-bit register (Q81. Q82 and Q83) uses a second I^2C bus (SC2 and SD2) to minimise noise. The register outputs control IF filter selection, battery charging and power switching, mode selection, RF attenuator, RF pre-amp, local oscillator range switching, AGC speed and the aux relay.

- It monitors and drives the RS232 data lines through Q2, Q3 and Q4 - RXD and TXD.

- It accepts data from both front and rear Infra Red sensors (Q1 and Q79) - IRR and IRF.

- It controls the carrier and local DDS IC's Q47 and Q48 on the serial bus - CLK, DAT, STC and STL

- It accepts data from the mute (MUT) and PLL unlock (PLK) lines through Q4A.

- The CPU clock is fed from the TCXO reference oscillator on pin 19 - XTAL1.

The CPU is powered from the +5C line and a reset pulse is applied at switch on through C10 to the RST pin. B1, the backup battery, supplies the RTC/RAM (Q6) whilst the set is not powered. The real time clock (RTC) uses a 32.768kHz xtal (X1) which can be trimmed by TC1. The memory organisation and RS232 control protocol is detailed in the computer remote control document.

6) Notch / Noise Blanker

6.1 Power Supply

There are two supply lines on the board. The logic control uses the +5C connection to the control unit, this is a permanently active, unswitched 5V supply. The remainder of the board uses an 8V supply regulated by Q7 from the B+ line and a low current 4V feed derived from a potential divider R21/R22 off the 8V supply.

6.2 Control Logic

Q1 and Q2 (PCF8574T) are 8-bit I/O expanders running off the I^2C bus SC1 and SD1. Q1 provides a D/A derived voltage, combined through R1-R4 to alter the noise blanker threshold level on pin 6 Q19B. Q2 provides various switching lines used by both the notch and noise blanker. Q5 (HSP45102) is a 12-bit numerically controlled oscillator. This also runs off the I^2C bus and provides the notch reference frequency. It runs at 100 times the audio notch frequency and feeds Q10 and Q13. It's clock is provided by xtal oscillator X1 and Q4.

6.3 Notch Filter

The audio path is broken within the microprocessor controlled audio pre-amp Q38. AOL feeds audio through Q19A into the first notch circuit Q10B, an LTC1060 dual switched capacitor filter. The audio then passes through Q9A to the second notch circuit Q13, a single switched capacitor filter. Audio returns to the main board via AIL after passing through Q9B. The cascaded pair of notch filters gives the notch filter it's specified high performance depth. The notch filter is switched in and out of circuit by Q6C. Q10A in combination with an output from Q10B allows the auto notch tracking facility by comparing phase differences in Q11, Q12 and Q3B/C feeding the resulting control voltage SIG into the spare pin 1 on Q9 on the control unit.

6.4 Noise Blanker

The IF signal at IF2 is buffered by Q15 before being fed into Q14 (SA614A) a monolithic low power FM IF system with RSSI. The RSSI output is fed into Q18 (4528), the blanking level being determined by Q19B. The two switchable widths of blanking pulses are produced by Q18A/Q18B and fed into the AGC system to momentarily desensitise the receiver during the noise pulse period. In AM mode the audio is also muted by a signal fed into the gate of Q8.

7) Battery Option

The battery option centres around Q2, a MAX1771E DC-DC controller, Q3 an MPT3055 FET and a 12V sealed lead acid cell. Two rates of charge are available, switched by the CHG line. This is timed from the microprocessor. and switches Q1. The battery is protected by fuse F1 and the charge circuit is temperature compensated by TH1.

AR7030 Spurii List

Every complex receiver generates internal signals that are received by the receiver itself and appear as small whistles or unmodulated carriers on the recovered audio. These are known as spurii or birdies. The following list shows spurii found on typical, fully cased AR7030's with antenna connections terminated into a 50 ohm dummy load. Whilst trying to ensure that the list is accurate and comprehensive we cannot guarantee that it is definitive and the number and level of spurii may vary slightly from set to set. We must therefore stress that any further spurii you may find that are not documented on this list do not constitute a fault condition.

The first column shows the frequency - this can vary with mode, differ slightly between sets and may be temperature dependant.
The second column shows the signal strength measured on the S-meter and is shown as the S point + 1dB increments. No level indicates that the spurious was below the S-meter threshold.
The third column shows the difference to the S-meter reading when the pre-amp is activated - in many cases the spurii level actually falls, again no level indicates that the spurious was below the S-meter threshold.

As an indication S1 is approximately equal to -113dBm or 0.5uV

Frequency	S-meter	Pre-amp +10dB
630 kHz		
750 kHz		
945 kHz		
1120 kHz		
1249 kHz		
1492 kHz		
1.8559 MHz		
1.8680 MHz		
2.2136 MHz		
2.2340 MHz		
2.4417 MHz		
2.4849 MHz		
2.6050 MHz		
2.9760 MHz		
3.1036 MHz		
3.7240 MHz		
4.3420 MHz		
4.8836 MHz		
4.9596 MHz		
4.9976 MHz		
5.3399 MHz		
5.8420 MHz		
5.9724 MHz		
6.1970 MHz		
6.8156 MHz		
6.8917 MHz	S1+4	
7.0425 MHz	S2	
7.1190 MHz		
7.7797 MHz		
8.0087 MHz		
8.0509 MHz		
8.3594 MHz		
8.8986 MHz		
9.2801 MHz		
10.2204 MHz		
10.5256 MHz		
10.5638 MHz	S3+1	S1+4
10.5867 MHz		
10.6210 MHz		
10.7927 MHz	S3	S1+4
10.9072 MHz		
11.1362 MHz	S1+4	S5+2
12.2037 MHz		
12.3346 MHz		
13.5768 MHz		
14.2377 MHz	S1+2	
14.3140 MHz		
14.4667 MHz		
14.5430 MHz	S1+4	
15.0009 MHz	S6	S3+4
15.0412 MHz		
16.0174 MHz		
16.1319 MHz		
16.3608 MHz		
16.4753 MHz		
17.2684 MHz	S2+1	S1
17.4516 MHz	S2+1	S2
17.9498 MHz	S1+1	
18.2550 MHz		
18.9160 MHz		
19.6788 MHz		
20.4163 MHz		
21.3566 MHz		
21.5855 MHz		
21.6619 MHz		
21.7000 MHz		
21.9290 MHz		
22.0435 MHz		
22.2724 MHz	S1+4	
25.0564 MHz		
25.3740 MHz		
25.9845 MHz		
26.1774 MHz	S1+1	
26.3606 MHz		
26.9125 MHz		
27.0015 MHz		
27.1537 MHz		
27.8406 MHz		
29.0860 MHz	S1+4	
29.3913 MHz	S2+4	S1+4
30.0522 MHz		
30.2812 MHz		

AR7030 Test and Alignment Program.

Overview :-

This program is intended as a calibration and alignment aid for the AR7030 receiver. A calibrated signal generator, a frequency meter capable of measuring frequency and period and a digital voltmeter are required to carry out the alignment process. An oscilloscope or an RF voltmeter is useful for tuned circuit peaking. Additionally a high purity two-signal source is needed for the mixer bias adjustment and the correct trimming tools will reduce damage to coil cores.

The receiver under alignment should be operated under normal conditions with a 15V supply and at room temperature. A period of more than 10 minutes operation is recommended before any adjustments are made.

Signals for adjustment and calibration are all unmodulated with 50 ohms source impedance and should be fed into the 50 ohm antenna input, with the Antenna Select Switch set to the 50 ohm position.

For complete alignment, the program menus should be worked through in sequence. If a partial alignment is intended, beware that there are some inter-dependencies between adjustments. All sections of the program that over-write calibration data in the receiver's memory allow a get-out before new data is committed.

Adjustment accuracy :-

The calibration routines expect external signals to be accurate to within +/- 500Hz of the specified frequency and within +/- 1dB of level.

The frequency accuracy of the receiver is dependent on a frequency measurement of the local oscillator. The meter used for this measurement should have an inherent accuracy better than +/- 0.1ppm, and the adjustment accuracy should be better than +/- 30Hz. These limits will ensure that the receiver is accurate to +/- 0.5ppm.

The real time clock frequency is set with a period measurement of the 1Hz divided clock. Typically the period should be set to within +/- 4us of 1 second which will give a clock accuracy of +/- 10 seconds per month (not allowing for thermal effects).

Software Installation :-

The software comprises of a single file - 7030TEST.EXE It is DOS based and can be used on virtually all PC's and compatibles running DOS 3.3 or higher. The file should be copied to, and run from the hard drive although it will run from the floppy if necessary. The program does not support a mouse or pointing device and most instructions are intended to be carried out from the numeric keypad on the keyboard. The AR7030 should be connected to the computer RS232 port as detailed in the AR7030 operating manual using the specified lead.

Running the Software :-

Type **[7030TEST]** at the DOS prompt and the following opening screen should appear.

```
AR - 7030  Test and Alignment.    V3.1
==============================

Receiver type : Not Identified

      1)  Logon / Setup / Debug.
      2)  Frequencies.
      3)  Local oscillator.
      4)  Sync detector.
      5)  IF system and S-Meter.
      6)  Check RF stages.
      7)  Mixer.
      9)  Information.
      10) End program.

   Enter item number ?
```

As each menu item is completed a * or ** will appear alongside the item. An * indicates that the menu item has been partially completed and a double ** indicates that all the menu items have been fully completed. This is to give a quick visual indication of progress through the alignment procedure. In many of the menus some of the text appears in brackets (.....). This is to give on screen instruction as to the test and alignment points, method of alignment or hints and tips.

Before the AR7030 will accept any instructions you must log on by pressing number **[1]**, this will display the next screen.

```
LOGON / SETUP / DEBUG
=====================

Receiver type : Not Identified

      1)  Logon to receiver.
      2)  Preset and Test Memory.
      4)  Test Display and Controls.
      5)  Set Clock Time.
      6)  Interactive Monitor / Debugger.
      0)  Return to Main Menu.

   Enter item number ?
```

Pressing **[1]** will display the following screen.

```
LOGON / SETUP / DEBUG
=====================

Receiver type : Not Identified

      1)  Logon to receiver.
      2)  Preset and Test Memory.
      4)  Test Display and Controls.
      5)  Set Clock Time.
      6)  Interactive Monitor / Debugger.
      0)  Return to Main Menu.

   Enter item number ? 1

     Enter COM port to use for communication with the radio.
     1 or 2 ?
```

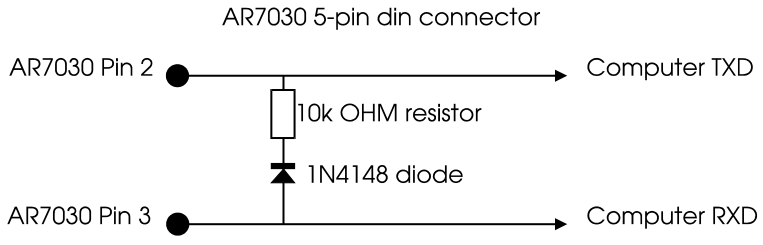
Press **[1]** or **[2]** to select the required COM port. Confirmation of correct logon will be confirmed by the message.

```
Receiver type : AR-7030 V*.* *
```

The numbers after the `V` indicate the software version, the letter `A` indicates a standard CPU, the letter `B` an enhanced CPU.

Once you have indicated which COM port you wish to use you will not be asked again until the program is re-run. This is useful if you are testing many radios. Alternatively you can add the COM port required as a command line option when starting the program - **[7030TEST 1]** selects COM port 1 and **[7030TEST 2]** selects COM port 2.

If at this point the unit fails to log on please check that the correct COM Port has been selected and that the connections between the computer and AR7030 are wired as per the details given in the operating manual. Some RS232 ports have been causing problems with the AR7030 remote facility as the negative line has not been pulling low enough. If you experience RS232 corruption problems and inconsistency, try adding a diode and resistor between Pin 2 and Pin 3 of the 5-pin DIN socket as shown below. Improved RS232 communications has been incorporated from March 97 on.



Pressing number **[2]** will preset all 100 memories (400 if enhanced B version processor with additional EEPROM) to 00.000 AM with standard default settings, preset all modes to default settings, load the default filter bandwidth settings, load the default S-Meter calibration data, load the default settings into the 3 setup memories A, B and C, checks the RTC/RAM, checks the EEPROM, (checks the additional EEPROM if fitted) and resets the unit to 7.100.00 AM with default settings etc. The following warning is displayed before you commit the action. Press **[1]** to continue or anything else to stop and return to previous menu.

```
******   WARNING   ******
```

```
  All S-Meter calibration data will be lost
  and any memory frequencies overwritten.

  Enter 1 to continue (or anything else to stop) ?
```

If an enhanced CPU is detected the menu includes an additional item -

```
      3)  Setup option information.
```

Press **[3]** to display the following.

```
SETUP RECEIVER OPTIONS
======================


      1)  Notch / Noise Blanker installed : YES
      2)  RF attenuator step 10dB   (DX)  : NO
      0)  Return to main menu.

   Enter item number ?
```

Press **[1]** to toggle the Notch / Noise Blanker installed : YES / NO. Press **[2]** to toggle the RF attenuator step size to 10 dB : YES / NO. This requires hardware support and is only available on the DX version - not yet available at time of writing. Press **[0]** or **<ENTER>** to return to the previous menu.

Pressing number **[4]** will initially clear the display for test purposes then produce the following screen and activate all segments of the LCD, giving a black display.

```
TEST DISPLAY AND CONTROLS
=========================


   All segments on LCD should be black.


   Buttons :-  Power    *    Volume     : -----*---------------
               Menu
               [*]      *    Spin wheel : ----------------*-----
               Memory
               RF-IF         Tuning     : ----------*----------
               Filter   *
               Fast
               Mode <
               Mode >   *

Press ENTER to continue
```

As each button is pressed `***` will appear alongside the button name, this will revert to a single `*` when the button is released allowing a quick visual check of previously activated buttons. The `*` on the `---------*---------` scale alongside the `Volume`, `Spin wheel` and `Tuning` control will move left and right to indicate clockwise and anticlockwise rotation of the controls. This completes testing of all front panel controls apart from the PHONES socket. Pressing **<ENTER>** returns you to the previous menu.

Pressing number **[4]** will set the receiver's internal real time clock to match the computer's clock and date. It is therefore important that your computer's clock and date is accurately set if you wish this operation to be worthwhile. The following screen is displayed.

```
LOGON / SETUP / DEBUG
=====================

Receiver type : AR-7030 V*.* *

      1)  Logon to receiver.
   *  2)  Preset and Test Memory.
   *  3)  Setup option information.
   *  4)  Test Display and Controls.
      5)  Set Clock Time.
      6)  Interactive Monitor / Debugger.
      0)  Return to Main Menu.

   Enter item number ? 5

Clock set to hh:mm:ss  mm-dd-yyyy

Press ENTER to continue
```

Pressing **<ENTER>** returns you to the menu.

Pressing number **[6]** selects the `Interactive Monitor / Debugger`, this displays the following

```
A R B U G Monitor     (Type ? for help)
=================

ARBUG>
```

Pressing **[?]** followed by **<ENTER>** displays the following

```
A R B U G Monitor     (Type ? for help)
=================

ARBUG>?
    a   set address              x   execute routine
    p   set page                 l   set lockout
    d   display bytes            k   set mask (B)
    m   monitor byte             b   operate button (B)
    s   monitor signal level     q   quit.
    w   write byte

ARBUG>
```

If at this point you do not understand what is displayed or you need to know anything else about the debugger we suggest that you leave it well alone. It allows you to write directly to the processor in Hex and any incorrect use will render the receiver inoperable! The routine was originally written by **JT** our design engineer during his prototyping and development of the AR7030 and we have never found it necessary to use it during normal servicing. Press **[q]** to quit then **[0]** or **<ENTER>** to return to the main menu

```
AR - 7030  Test and Alignment.    V3.1
==============================

Receiver type : AR-7030 V*.* * + NNB opt.

  *   1)  Logon / Setup / Debug.
      2)  Frequencies.
      3)  Local oscillator.
      4)  Sync detector.
      5)  IF system and S-Meter.
      6)  Check RF stages.
      7)  Mixer.
      8)  Notch filter
      9)  Information.
      10) End program.

   Enter item number ?
```

If the Notch / Noise blanker has been enabled in previous menu item `3)` the receiver type will now show as follows

```
Receiver type : AR-7030 V1.4 B + NNB opt.
```

and an additional item `8)` will appear in the main menu to align the notch filter. `(DX)` will appear in the `Receiver type` line if the 10dB attenuator option is enabled.

Press **[2]** to adjust the two reference frequencies and display the following.

```
ADJUST FREQUENCIES
==================


      1)  Adjust Reference Oscillator.
      2)  Adjust Clock.
   *  3)  Set Clock Time.
      0)  Return to Main Menu.

   Enter item number ?
```

Pressing **[1]** allows adjustment of the Reference Oscillator and displays the following screen.

```
ADJUST REFERENCE FREQUENCY
==========================


Local frequency        : 75.00000 MHz at TP7
(adjust Q45 TCXO)
Press ENTER to continue




Note:
If the frequency error is more than a few kHz then
it is possible that the local osc PLL is unlocked.
Adjust L50 / L51 for 14.0 to 14.3V on TP5.
```

Press **<ENTER>** to return to menu and press **[2]** to adjust the clock frequency and display the following screen.

```
ADJUST CLOCK FREQUENCY
======================


Clock period    : 1.00000 s pulse period at TP1
(adjust TC1)

Press ENTER to continue




Note:
Test point and adjustment are on front panel PCB.
```

Both these measurements should be carried after the unit has reached full operating temperature. Press **<ENTER>** to return to menu. Press **[3]** to set clock if necessary, this will already be marked done if it was carried out earlier in the procedures. Press **<ENTER>** to return to the main menu.

```
AR - 7030  Test and Alignment.    V3.1
==============================

Receiver type : AR-7030 V*.* *

  *   1)  Logon / Setup / Debug.
  **  2)  Frequencies.
      3)  Local oscillator.
      4)  Sync detector.
      5)  IF system and S-Meter.
      6)  Check RF stages.
      7)  Mixer.
      9)  Information.
      10) End program.

   Enter item number ?
```

Press **[3]** to align the local oscillator and display the following screen

```
ADJUST LOCAL OSCILLATOR
=======================


      1)  Local Osc range 1 high.
      2)  Local Osc range 1 low.
      3)  Local Osc range 2 high.
      4)  Local Osc range 2 low.
      5)  Local Osc range 3 high.
      6)  Local Osc range 3 low.
      7)  Local Osc range 4 high.
      8)  Local Osc range 4 low.
      0)  Return to main menu.

   Enter item number ?
```

Press **[1]** to initially align the VCO coils

```
Range 1 high           : TP5 Voltage 14.0 to 14.3V
(adjust L50 / L51)
```

Both L50 and L51 affect the alignment of the VCO, they should be adjusted in such a way that the desired voltage is achieved (14.0V to 14.3V) and the cores of the transformers are in a physically matched position i.e. the same insertion depth in the coil former. Menu items 2 to 8 should then be checked in sequence for correct TP5 voltage.

```
Range 1 low            : TP5 Voltage above 3V
(revise previous settings)

Range 2 high           : TP5 Voltage below 15V
(modify C153 / C161)

Range 2 low            : TP5 Voltage above 3V
(revise previous settings)

Range 3 high           : TP5 Voltage below 15V
(modify C154 / C162)

Range 3 low            : TP5 Voltage above 3V
(revise previous settings)

Range 4 high           : TP5 Voltage below 15V
(revise previous settings)

Range 4 low            : TP5 Voltage above 3V
(revise previous settings)
```

C153, C154, C161 and C162 are select on test (SOT) capacitors. These will have been selected during initial alignment during production and should never need changing. Press **[0]** or **<ENTER>** to return to the main menu.

```
AR - 7030  Test and Alignment.    V3.1
==============================

Receiver type : AR-7030 V*.* *

  *   1)  Logon / Setup / Debug.
  **  2)  Frequencies.
  **  3)  Local oscillator.
      4)  Sync detector.
      5)  IF system and S-Meter.
      6)  Check RF stages.
      7)  Mixer.
      9)  Information.
      10) End program.

   Enter item number ?
```

Press **[4]** to align the Sync detector and display the following screen

```
ADJUST SYNCHRONOUS DETECTOR
===========================


Phase null             : Zero volts between TP3 and TP4
(adjust VR2) (aim for below +/-10mV)


Press ENTER to continue
```

Pressing **<ENTER>** changes the display to this :-

```
ADJUST SYNCHRONOUS DETECTOR
===========================


VCO centre             : Zero volts between TP3 and TP4
(adjust VR3) (aim for below +/-30mV)
(ensure audio output is at zero beat)

Press ENTER to continue
```

These adjustments should be carried out with the unit at full operating temperature. Ideally a DVM should be used and the presets locked with locking compound once the adjustment is complete. Press **<ENTER>** to return to the main menu.

```
AR - 7030  Test and Alignment.    V3.1
==============================

Receiver type : AR-7030 V*.* *

  *   1)  Logon / Setup / Debug.
  **  2)  Frequencies.
  **  3)  Local oscillator.
  **  4)  Sync detector.
      5)  IF system and S-Meter.
      6)  Check RF stages.
      7)  Mixer.
      9)  Information.
      10) End program.

   Enter item number ?
```

Press **[5]** to align the IF, calibrate the S-Meter, edit the S-Meter cal values and display the following screen.

```
ADJUST IF AND S-METER
=====================


      1)  Align IF System.
      2)  Calibrate S-Meter.
      3)  View / Edit S-Meter Cal values.
      0)  Return to Main Menu.

   Enter item number ?
```

```
Note:
IF mixer adjustment has not been performed, then
ensure that mixer bias pot VR1 is set to mid-position
```

Press **[1]** to align the IF System and display the following screen.

```
ALIGN IF SYSTEM
===============


HET tune              : Max 44.5MHz signal at TP2
(adjust TC2)



Apply signal to antenna input  : 7.1MHz at -90dBm

IF tune : Max signal strength  : 92 ***:****:****:****:***
(adjust L26)



Press ENTER to continue
```

Align TC2 for maximum Het injection at TP2 (pin 5 Q20), expect between 0.5V and 1.0V p-p on an oscilloscope. If this level cannot be achieved increase R152 to 2k2 in the Het Multiplier.
Align L26 for maximum signal strength reading. This is the only adjustable IF transformer in the set and has a fairly flat response. To achieve an exact peak point it is sometimes easier to increase or decrease the SSG output slightly to move towards a threshold point of a * on the bar graph or digit on the numeric indication. The bar graph and numeric indication are directly linked, use which ever you find easiest. The indicated number is fairly meaningless other than it is a figure that is returned from the A/D converter out of the AGC system. At the time of writing this document with the software version 1.2 a reading of **89** to **95** would be considered normal but this may change with later production runs and software revisions. The final reading you achieve is only designed to indicate the peak alignment and is not written to the microprocessor so don't worry about the exact SSG output. Press **<ENTER>** to return to the previous menu and press **[2]** to calibrate the S-Meter and display the following screen.

```
CALIBRATE S-METER
=================


Apply signal to antenna input  : 7.1MHz at -113dBm


Meter point S1       Signal : 60 ***:****:*


Press ENTER when signal strength is stable
```

Inject SSG and press **<ENTER>** when signal strength is stable and to display the next screen. Reduce the SSG output as instructed on the screen and press **<ENTER>**. Repeat this several times until you see the following screen.

```
CALIBRATE S-METER
=================


Apply signal to antenna input  : 7.1MHz
(adjust level for zero error)

Cal marker level error   :    9+   -------------------*-
                                                    ^

Press ENTER when error is zero
```

Adjust output from SSG for zero error i.e. when the * sits above the ∧ or the numeric indicator shows 0 and press **<ENTER>** to display the next screen

```
CALIBRATE S-METER
=================


Applied signal   :  Reduce level by 10dB


Press ENTER to continue
```

Reduce SSG output by 10dB and press **<ENTER>** to display the next screen

```
CALIBRATE S-METER
=================


Applied signal   :  Reduce level by 10dB


Applied signal   :  Reduce level by a further 10dB


Press ENTER to continue
```

Reduce SSG output by 10dB and press **<ENTER>** to display the next screen, this will now display the S-Meter calibration table.

```
CALIBRATE S-METER
=================


      1)  Cal value for S1 point     61
      2)  Step advance for S3        12
      3)  Step advance for S5        16
      4)  Step advance for S7         8
      5)  Step advance for S9         9
      6)  Step advance for S9+10      8
      7)  Step advance for S9+30     30
      8)  Step advance for S9+50     14
      9)  Filter cal 20dB ref        20
     10)  Filter cal 6dB ref          4

     11)  Exit to menu WITHOUT saving values
      0)  Update receiver and exit to menu

   Enter item number ?
```

The table shows typical cal values. Pressing **[1]** to **[8]** will allow editing of the relevant cal value, this is not normally necessary unless you require an alternatively calibrated S-Meter. If when the filters are calibrated, the values want nudging slightly up or down to give a more even spread of bandwidths, alter the Filter cal 6dB ref **[10]** up or down to 3 or 5 and re-cal the filters.
Pressing **[11]** returns to the previous menu without saving the cal values. The S-Meter would use the default values in this case or the previously stored values. The default values give a reasonable S-Meter indication but is not accurate for a given signal input.
Pressing **[0]** or **<ENTER>** stores the cal values and returns to the previous menu.

```
ADJUST IF AND S-METER
=====================


   *  1)  Align IF System.
   *  2)  Calibrate S-Meter.
      3)  View / Edit S-Meter Cal values.
      0)  Return to Main Menu.

   Enter item number ?




Note:
IF mixer adjustment has not been performed, then
ensure that mixer bias pot VR1 is set to mid-position
```

Pressing **[3]** loads the cal table out of the receiver and allows editing of the cal values as previously described.
Pressing **[0]** returns to the main menu.

```
AR - 7030  Test and Alignment.    V3.1
==============================

Receiver type : AR-7030 V*.* *

  *   1)  Logon / Setup / Debug.
  **  2)  Frequencies.
  **  3)  Local oscillator.
  **  4)  Sync detector.
  **  5)  IF system and S-Meter.
      6)  Check RF stages.
      7)  Mixer.
      9)  Information.
      10) End program.

   Enter item number ?
```

Press **[6]** to check the RF stages and display the next screen.

```
RF STAGE CHECK
==============


      1)  Check attenuator and pre-amplifier.
      2)  Check RF filters.
      0)  Return to Main Menu.

   Enter item number ?
```

Press **[1]** to check the attenuator and pre-amplifier and display the following screen.

```
CHECK ATTENUATOR AND PRE-AMPLIFIER
==================================


Apply signal to antenna input  : 7.1MHz at -40dBm


Press ENTER when signal is present
```

Apply signal and press **<ENTER>** to display the following screen

```
CHECK ATTENUATOR AND PRE-AMPLIFIER
==================================


Apply signal to antenna input  : 7.1MHz at -40dBm


Checking levels ...

Preamplifier Gain     :   +10dB
1st step attenuator   :   -10dB
2nd step attenuator   :   -20dB
3rd step attenuator   :   -30dB
4th step attenuator   :   -40dB

Press ENTER to continue
```

An error of 2dB is normal and acceptable, sometimes the 1st step attenuator may have a 3dB error, again this is nothing to worry about. Press **<ENTER>** to return to the previous menu then press **[2]** to check the RF filters and display the next screen.

```
CHECK RF FILTERS
================


Apply signal to antenna input  : 7.1MHz at -40dBm


Press ENTER when signal is present
```

Apply signal and press **<ENTER>** to display the following screen.

```
CHECK RF FILTERS
================


Apply signal to antenna input  : 29.9MHz at -40dBm


Press ENTER when signal is present
```

Apply signal and press **<ENTER>** to display the following screen.

```
CHECK RF FILTERS
================


Apply signal to antenna input  : 500kHz at -40dBm


Press ENTER when signal is present




High frequency level change   :   +0dB
```

Apply signal and press **<ENTER>** to display the following screen.

```
CHECK RF FILTERS
================


Apply signal to antenna input  : 1.7MHz at -40dBm


Press ENTER when signal is present




High frequency level change   :   +0dB
Low frequency level change    :   +0dB
```

Apply signal and press **<ENTER>** to display the final screen

```
CHECK RF FILTERS
================


Apply signal to antenna input  : 1.7MHz at -40dBm


Checking level ...



High frequency level change   :   +0dB
Low frequency level change    :   +0dB
High-pass filter level change :   +0dB
Low-pass filter level change  :   +0dB

Press ENTER to continue
```

This shows the error in dB's of the frequency response of the front end filters referenced to the S-Meter which is calibrated at 7.1MHz. It also therefore shows the sensitivity of the set referenced to the S-Meter cal table. An error of 3dB is normal, occasionally you may observe 4dB error, again this is nothing to worry about and is simply due to component tolerances. Anything more than 4dB would possibly indicate a fault. Press **<ENTER>** to return to the main menu.

```
AR - 7030  Test and Alignment.    V3.1
==============================

Receiver type : AR-7030 V*.* *

  *   1)  Logon / Setup / Debug.
  **  2)  Frequencies.
  **  3)  Local oscillator.
  **  4)  Sync detector.
  **  5)  IF system and S-Meter.
  **  6)  Check RF stages.
      7)  Mixer.
      9)  Information.
      10) End program.

   Enter item number ?
```

Press **[7]** to align the mixer, measure the IP2 and IP3 values and display the following screen.

```
ADJUST MIXER BIAS
=================


Apply two signals    :  11.000MHz AND 11.060MHz each at 0 dBm
(adjust VR1 for lowest IM product levels)


Worst case IMD3 level  : 112 112   **:****:****:****:****:**

Sum frequ IMD2 level   :      94   **:****:****:**


Calculated values :  IP3 = +34dBm      IP2 =  +86dBm
(calculated intercept point values
 assume that the S-Meter is calibrated)

Press SPACE to select IMD3 for rapid update
Press ENTER when adjustment is complete
```

Typical values are shown in the above screen. On initial start-up this test will measure the cal values for both IMD2 and IMD3 and calculate them as IP2 and IP3 dBm values. The IMD2 level will then remain active allowing alignment of VR1. Approximately every 10 sec's it will switch to measure the IMD3 and return to active IMD2 measurement thus updating the IP3 calculated value. If **<SPACE>** is pressed the procedure is reversed i.e. IMD3 remains active and the unit will switch to measure IMD2 every 10 sec's. Alignment of VR1 should achieve an IP3 value of between +30dBm and +35dBm and an IP2 value of anywhere between +75dBm and +110dBm. The dip for IP2 and IP3 does not generally occur in the same place on the preset and a compromise has to be made in the alignment to achieve the specification.

Press **<ENTER>** to return to the main menu.

```
AR - 7030  Test and Alignment.    V3.1
==============================

Receiver type : AR-7030 V*.* * + NNB opt.

  *   1)  Logon / Setup / Debug.
  **  2)  Frequencies.
  **  3)  Local oscillator.
  **  4)  Sync detector.
  **  5)  IF system and S-Meter.
  **  6)  Check RF stages.
  **  7)  Mixer.
      8)  Notch Filter.
      9)  Information.
      10) End program.

   Enter item number ?
```

Press [8] to align the notch filter and display the following screen

```
ADJUST NOTCH FILTER
===================


Turn Notch VR2 fully CCW.

Monitor receiver output with APM or voltmeter.
Adjust volume control to suitable level now.


Press ENTER to continue
```

The receiver at this point should produce a tone at approx. 2.5kHz. The volume control now needs to be advanced to an almost unbearable setting of about 80%. This is to give the required audio range to align the notch in the next stage of the alignment. Connect an audio power meter or voltmeter to the external speaker socket and press **<ENTER>** to reduce the audio level and display the next screen.

```
ADJUST NOTCH FILTER
===================


First notch pole      :  Minimum signal output.
(use + and - keys)

Notch Frequency = 2500 Hz

Press ENTER when adjustment complete.
```

Use the **[+]** and **[-]** keys on the computer keyboard to tune the notch filter to produce minimum audio output on the audio power or volt meter. The sensitivity of this meter will need to be increased to correctly measure this first notch pole. Press **<ENTER>** when the adjustment is complete and to move to the next screen.

```
ADJUST NOTCH FILTER
===================


First notch pole      :  Minimum signal output.
(use + and - keys)

Notch Frequency = 2500 Hz

Second notch pole     :  Minimum signal output.
(adjust Notch VR2)

Notch tracking phase  :  2.5V +/-0.5V on Notch TP2.
(adjust Notch VR1)


Press ENTER to continue
```

Adjust VR2 to produce minimum audio output on the audio power or volt meter, this aligns the second notch pole. Using a DVM adjust the notch tracking phase by aligning VR1 to produce 2.5V +/-0.5V on TP2. This completes the alignment of the notch filter. Press **<ENTER>** to return to the main menu.

```
AR - 7030  Test and Alignment.    V3.1
==============================

Receiver type : AR-7030 V1.4 B + NNB opt.

  *   1)  Logon / Setup / Debug.
  **  2)  Frequencies.
  **  3)  Local oscillator.
  **  4)  Sync detector.
  **  5)  IF system and S-Meter.
  **  6)  Check RF stages.
  **  7)  Mixer.
  **  8)  Notch Filter.
      9)  Information.
      10) End program.

   Enter item number ?
```

Press **[9]** to display the opening text from this document and finally press **[10]** to exit from the program.

Some parts of the program are linked, for example if the clock is set in the Logon / Setup / Debug menu the program will show that it has been set in the Frequencies menu thus reminding you. If the S-Meter has not been calibrated you will be reminded in the Check RF stages and Mixer menus that the calculated figures may not be accurate.

Battery Option

To set the charge voltage, substitute the battery for a high wattage resistor of approx. 50 ohm resistance. Adjust VR1 on the battery option PCB to give between 13.5-13.6V on trickle charge and check that this rises to approx. 14.5V on fast charge. This adjustment should be carried out at 20^0C. The trickle voltage at 30^0C is approx. 13.3V and at 10^0C, 13.8V.

If you have any servicing problem just give us a ring and we will be happy to try and help you; however a basic understanding of service techniques and test equipment is required before any service work is undertaken.

Specification subject to change due to continuous development of the receiver. E&OE.